

AU OPTRONICS CORPORATION

Product Specification

12.1” WXGA Color TFT-LCD Module

Model Name: B121EW02 V1

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Customer	Checked & Approved by

Product Specification

12.1" WXGA Color TFT-LCD Module
Model Name: B121EW02
V.1

Preliminary Specifications
 Final Specifications

Note: This Specification is subject to change without notice.

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2005/07/20	All	First Edition for Customer		
0.2 2006/01/06	6.7.16	Brightness tolerance +/-10%	Brightness tolerance +/-15%	



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2. General Description

B121EW02 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter card of backlight is not included.

B121EW02 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	307.9 (12.1W")
Active Area	[mm]	261.12(H) X 163.2(V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.204X0.204
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m ²]	200 typ. (5 points average) 170 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ.
Optical Rise Time/Fall Time	[msec]	10/15 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	5W max. (EBL 3W)
Weight	[Grams]	295g typ. 310g max
Physical Size	[mm]	275.82x 178 x 5.5 max.5.5max
Electrical Interface		1 channel LVDS
Surface Treatment		Glare, Harness 2H, Haze 25%, Reflectance 4.3%
Support Color		Native 262K colors (RGB 6-bit data driver)

Product Specification

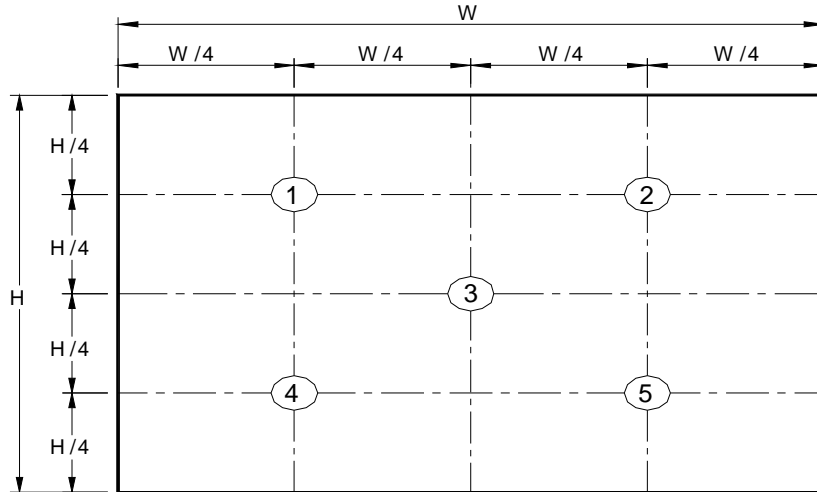
Temperature Range Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-40 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

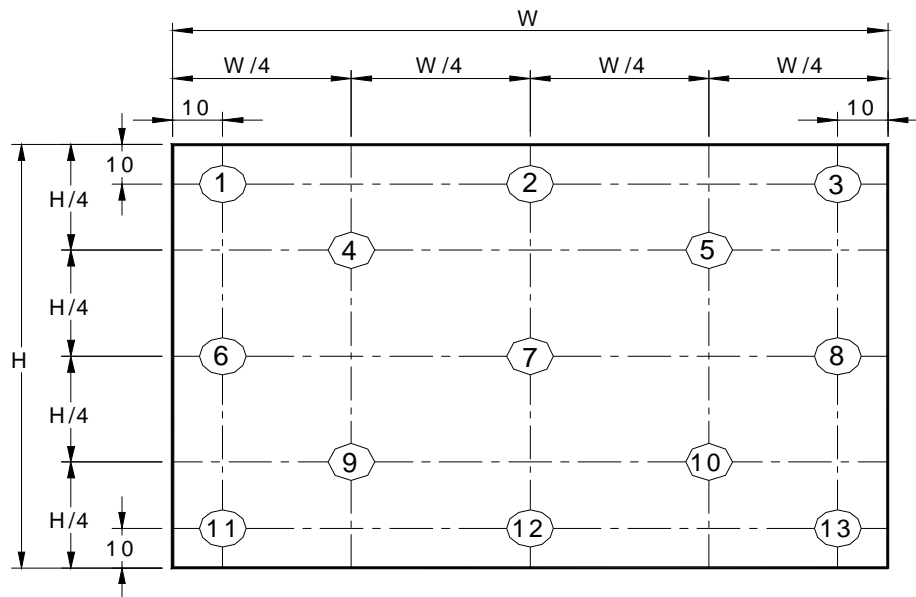
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance CCFL 6.0mA	[cd/m ²]	5 points average	170	200	-	1,2,3
Viewing Angle	[degree]	Horizontal (Right)	-	60	-	2,7
	[degree]	CR = 10 (Left)	-	60	-	
	[degree]	Vertical (Upper)	-	50	-	
	[degree]	CR = 10 (Lower)	-	50	-	
Uniformity		5 Points			1.25	1
Uniformity		13 Points			1.6	
CR: Contrast Ratio			350	400	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	10	15	5
	[msec]	Falling	-	15	20	
	[msec]	Raising + Falling		25	35	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.564	0.594	0.624	2,7
		Red y	0.305	0.335	0.365	
		Green x	0.298	0.328	0.358	
		Green y	0.501	0.531	0.561	
		Blue x	0.122	0.152	0.182	
		Blue y	0.113	0.143	0.173	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 261.12mm x 163.2mm)



Note 2: 13 points position



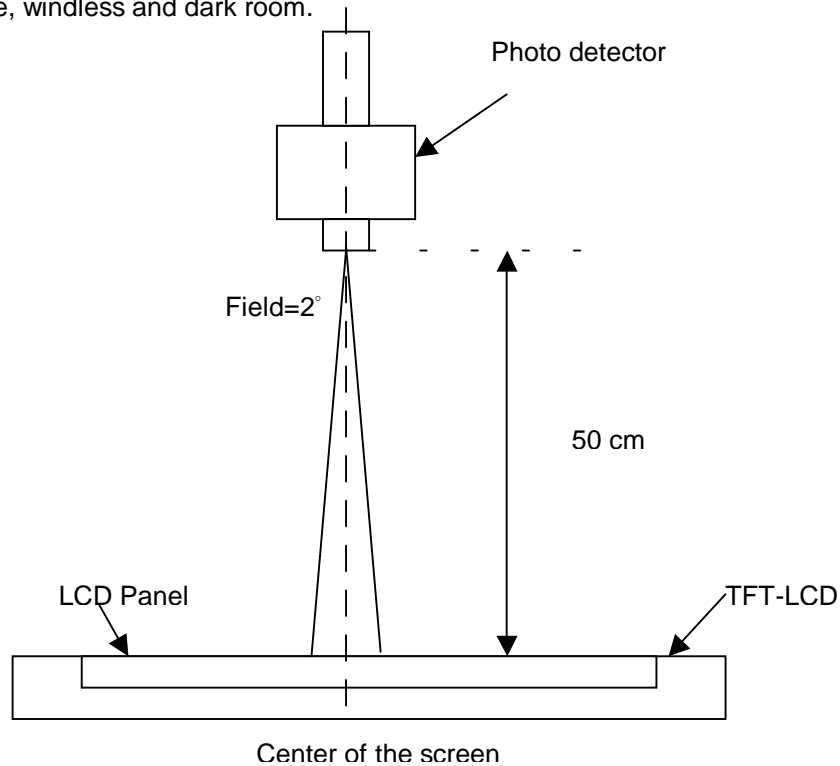
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



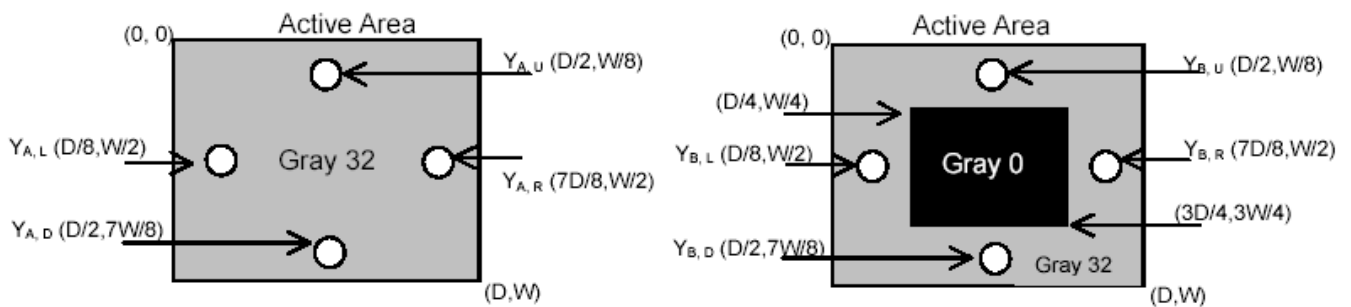
Note 5 : Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

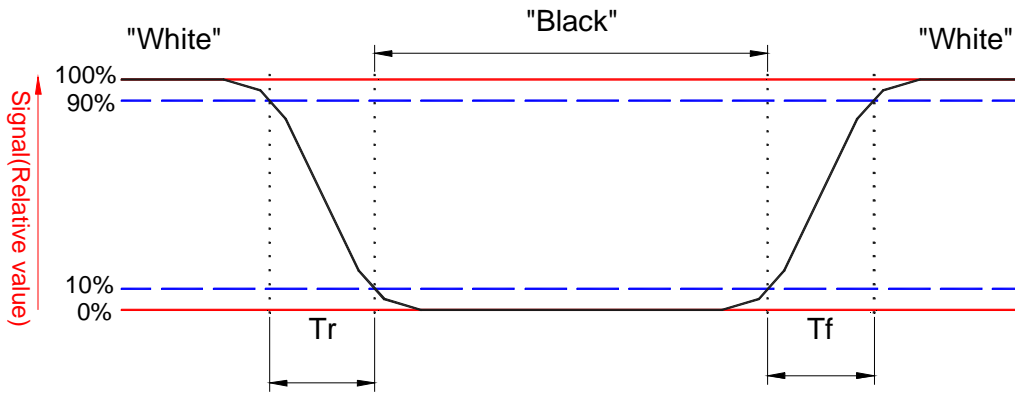
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



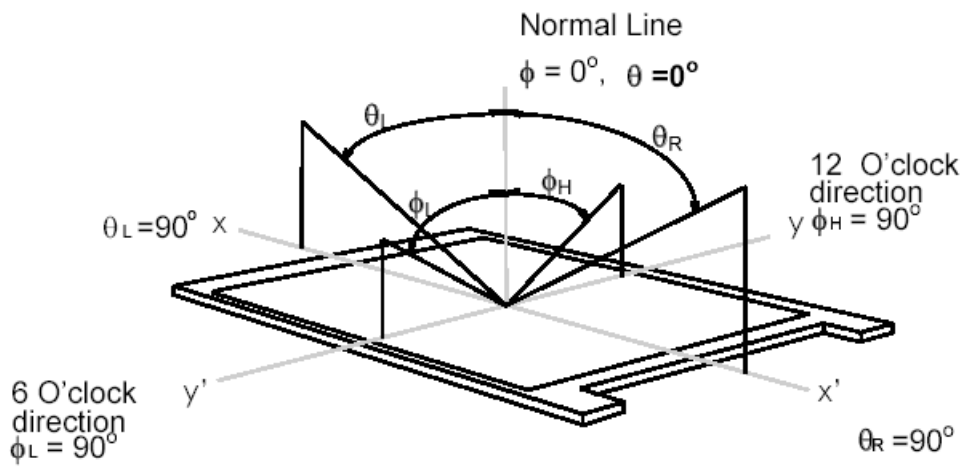
Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



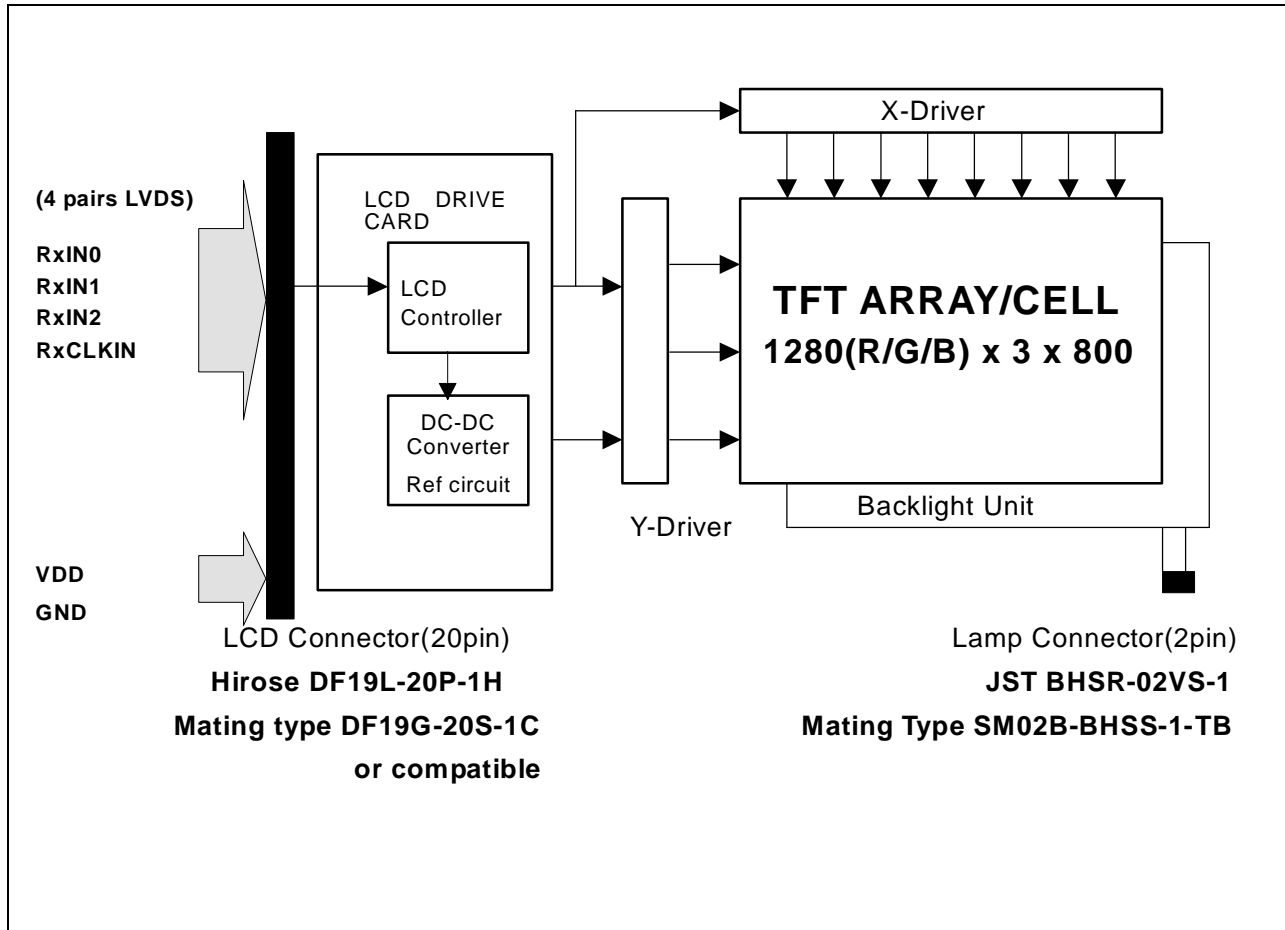
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	-	7	[mA] rms	Note 1,2

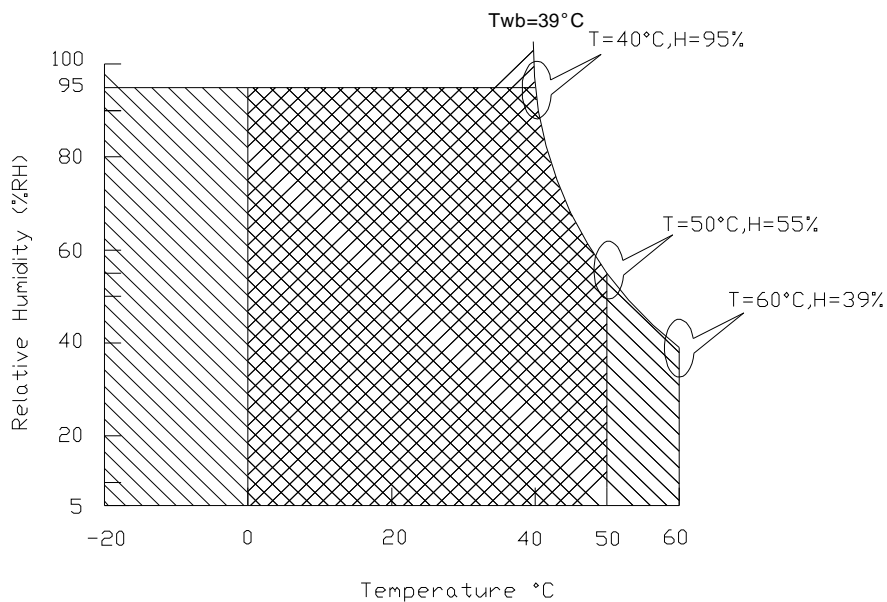
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-40	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

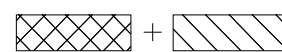
Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range



5. Electrical characteristics

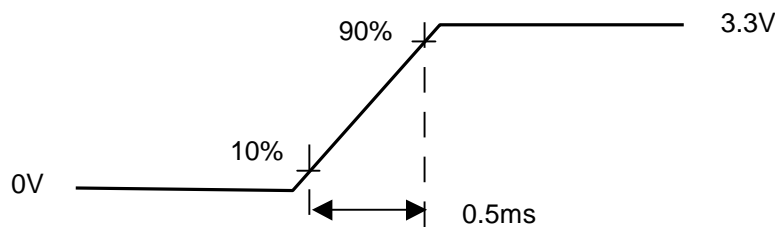
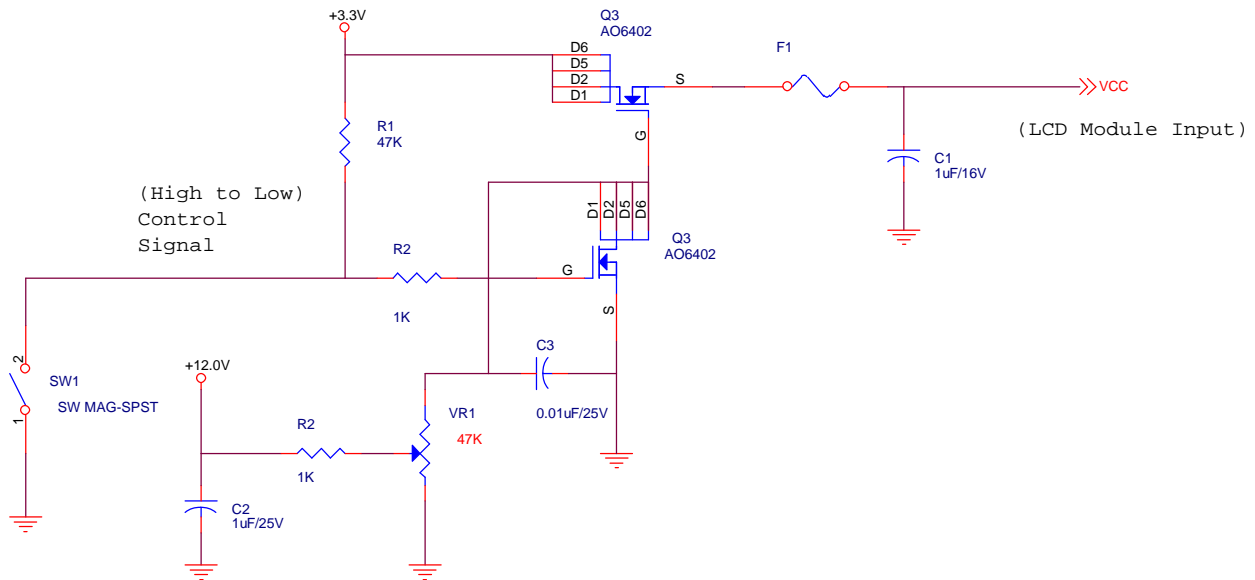
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	Volt	Load Capacitance 20uF
PDD	VDD Power	-	1.0	-	Watt]	Max:All Black Pattern
IDD	IDD Current	-	303	-	mA	Max:All Black Pattern
IRush	Inrush Current	-	-	1800	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	500	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise	-	-	100	[mV] p-p	

Note 1 : Measurement conditions:



Vin rising time

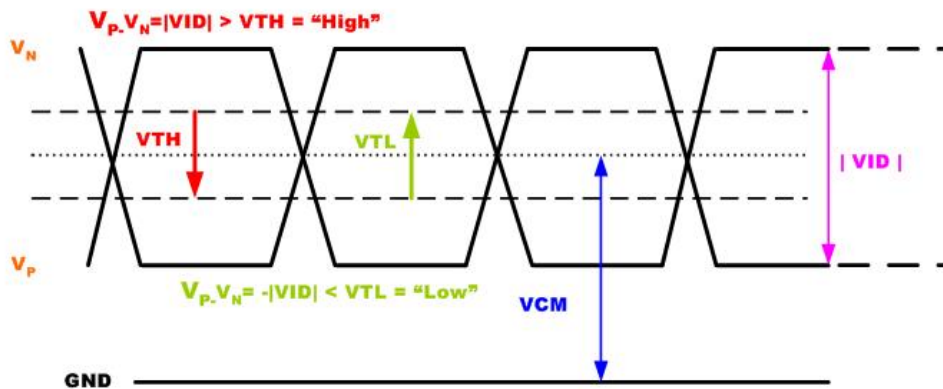
5.1.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off. It is recommended to refer the specifications.

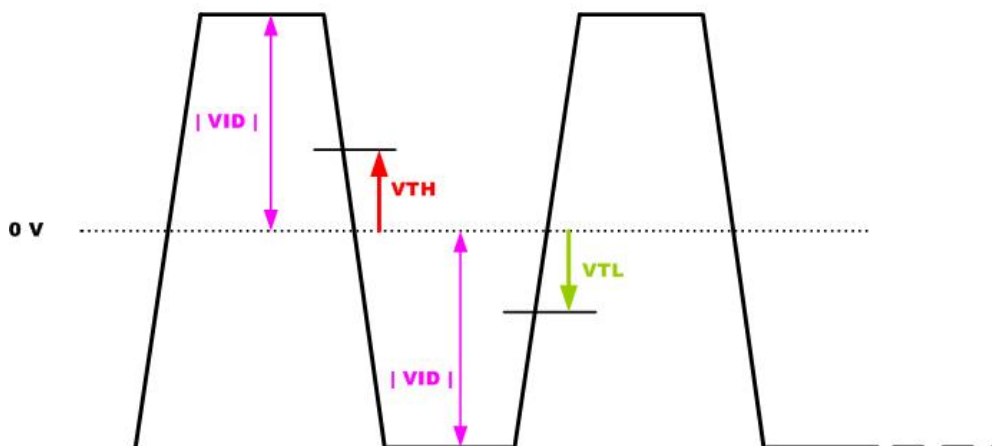
Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input voltage	VID	0.1	-	0.6	V	
LVDS input common mode voltage	VCM	1	1.2	1.5	V	VTH/VTL=+-100mV
Differential Input High Threshold Voltage	VTH	-	-	100	mV	VCM=1.2V
Differential Input Low Threshold Voltage	VTL	-100	-	-	mV	

Note: LVDS Signal Waveform

Single-end Signal



Differential Signal



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	170	200	-	[cd/m ²]	(Ta=25°C)
CCFL current(ICFL)	5.5	6.0	6.5	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(FCFL)	50	60	70	[KHz]	(Ta=25°C) Note 3,4
CCFL Ignition Voltage(Vs)	1400	-	-	[Volt] rms	(Ta= 0°C) Note 5
CCFL Voltage (Reference) (VCFL)	-	580	-	[Volt] rms	(Ta=25°C) Note 6
CCFL Power consumption (PCFL)	-	3.5	-	[Watt]	(Ta=25°C) Note 6

Note 1: Typ are AUO recommended Design Points.

- *1 All of characteristics listed are measured under the condition using the AUO Test inverter.
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
- *4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
- *6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

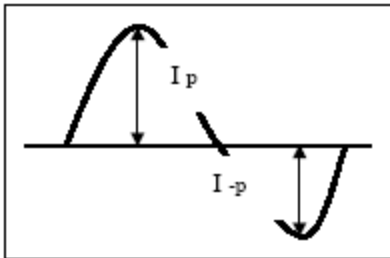
Note 6: Calculator value for reference (ICFL×VCFL=PCFL)

Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

- a. The asymmetry rate of the inverter waveform should be less than 10%.
- b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.

* Inverter output waveform had better be more similar to ideal sine wave.



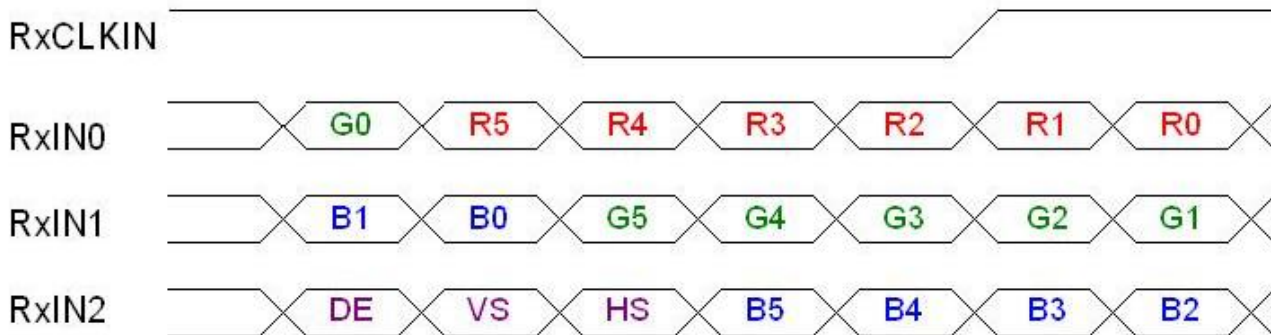
* Asymmetry rate:

$$\frac{|I_p - I_{-p}|}{I_{rms}} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data.
DE	Display Timing	When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	Vertical synchronized signal
HS	Horizontal Sync	Horizontal synchronized signal

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

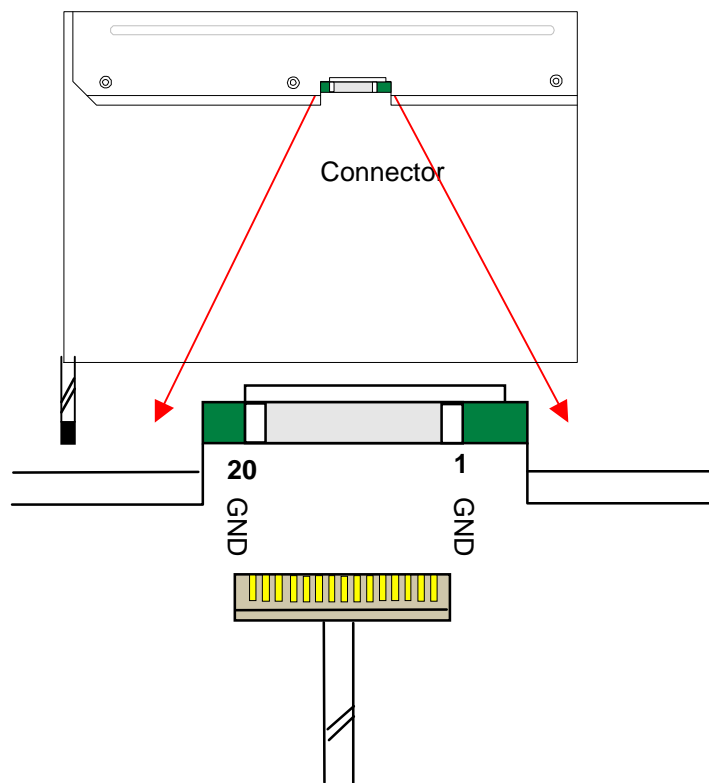
6.3 Signal Description

Signal Name	Description
RxIN0N, RxIN0P	LVDS differential data input (R0~R5, G0)
RxIN1N, RxIN1P	LVDS differential data input (G1~G5, B0~B1)
RxIN2N, RxIN2P	LVDS differential data input (B2~B5, Hsync, Vsync, DE)
RxCLKINN, RxCLKINP	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

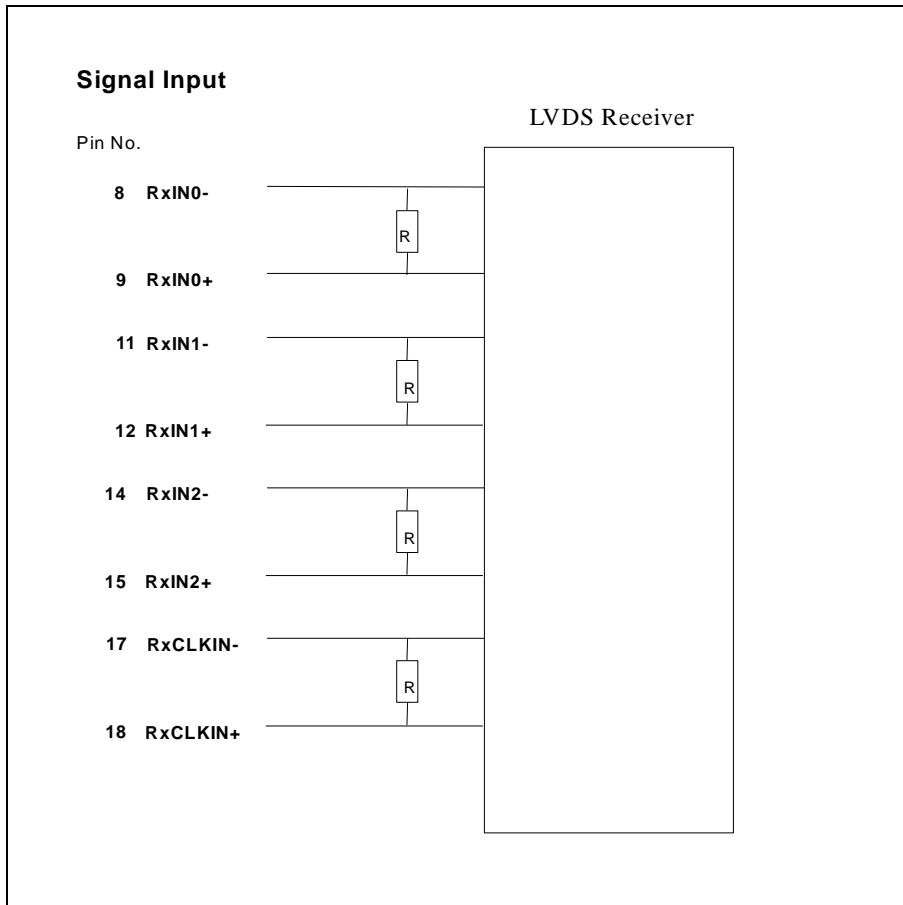
Note1: Start from right side

Note2: Please follow VESA.

Note3: Input signals shall be low or Hi-Z state when VDD is off. Internal circuit of LVDS inputs are as following.



The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

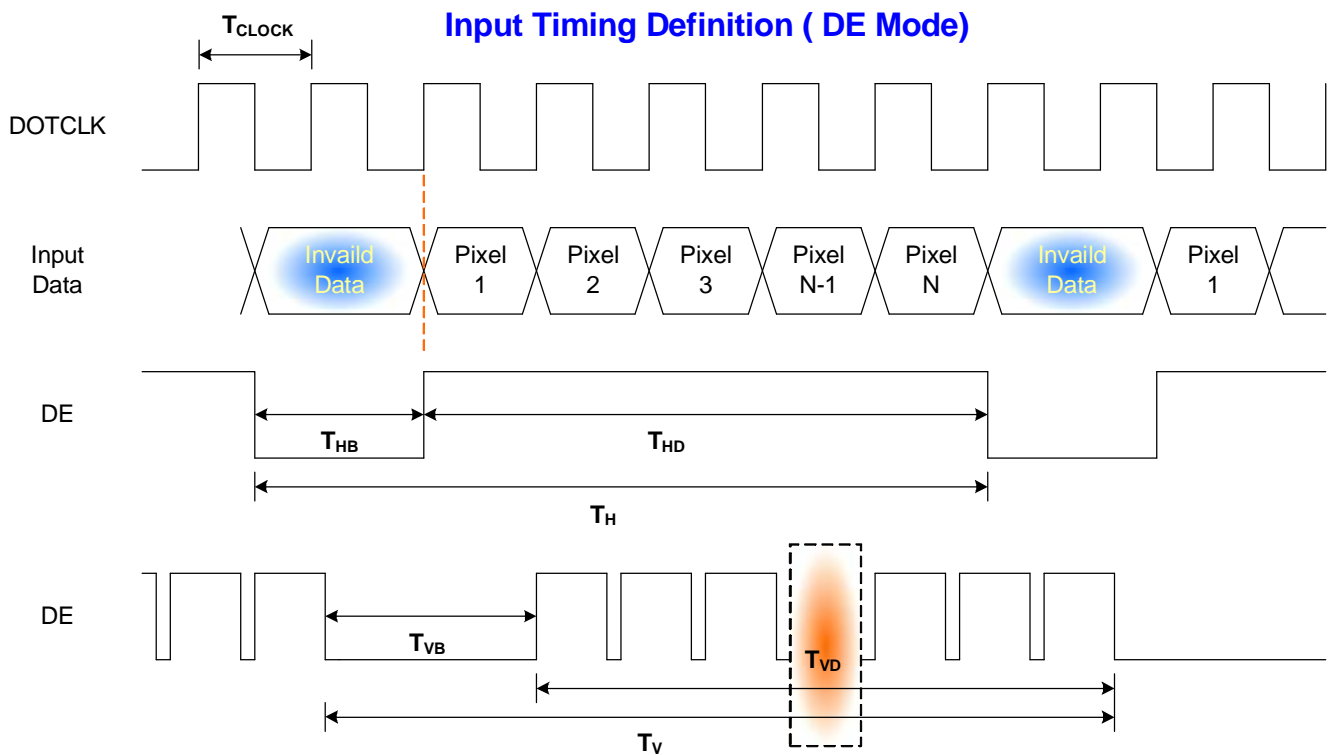
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{\text{Clock}}$	62	68.9	75	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	128	420	

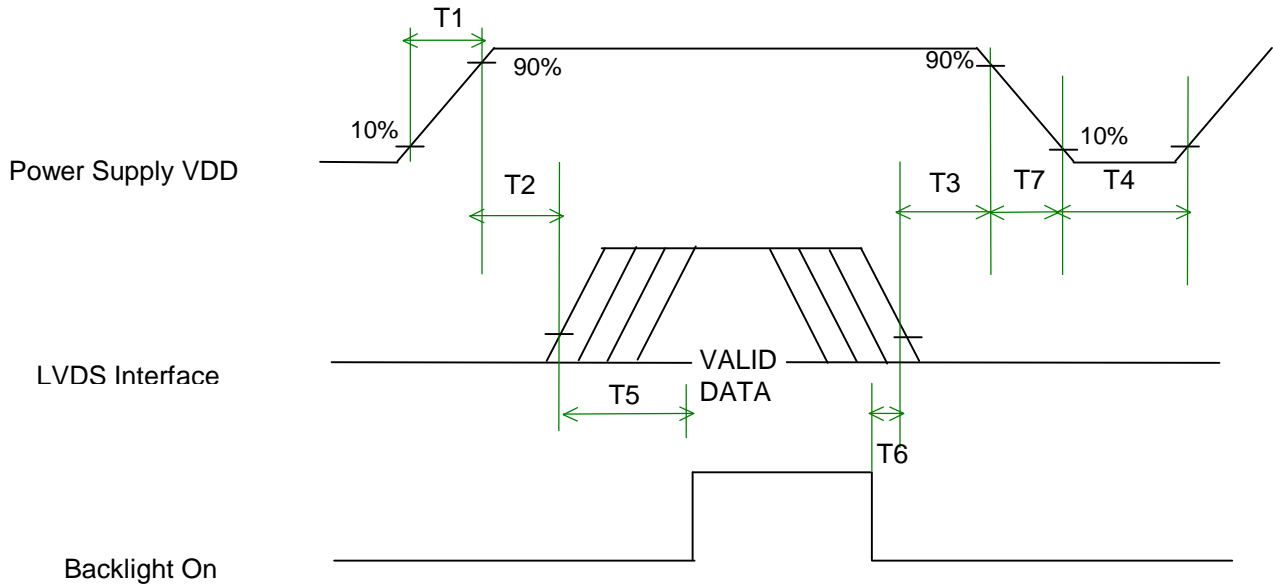
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	500	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

(A) CONNECTOR

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	DF19L-20P-1H
Mating Housing/Part Number	DF19G-20S-1C or compatible

(B) Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VDD _{EDID}
5	AGING	6	CLK _{EDID}
7	DATA _{EDID}	8	RxIN0N
9	RxIN0P	10	GND
11	RxIN1N	12	RxIN1P
13	GND	14	RxIN2N
15	RxIN2P	16	GND
17	RxCLKINN	18	RxCLKINP
19	GND	20	GND

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 1.5G
- I Frequency: 26 - 500Hz Random
- I Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- I Test method: Non-Operation
- I Acceleration: 220 G , Half sine wave
- I Active time: 2 ms
- I Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40°C/95%,250Hr	
High Temperature Operation	50°C/Dry,250Hr	
Low Temperature Operation	0°C,250Hr	
On/Off Test	ON/30 sec. OFF/30sec., 30,000 cycles.	
Hot Storage	65°C/20% RH ,250 hours	
Cold Storage	-40°C/50% RH ,250 hours	
Thermal Shock Test	-40°C/20 min ,65°C/20 min 50cycles	
Hot Start Test	50°C/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0°C/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	220G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.5 G zero-to-peak, 26 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25°C , 2000hours, Operating with loop pattern	

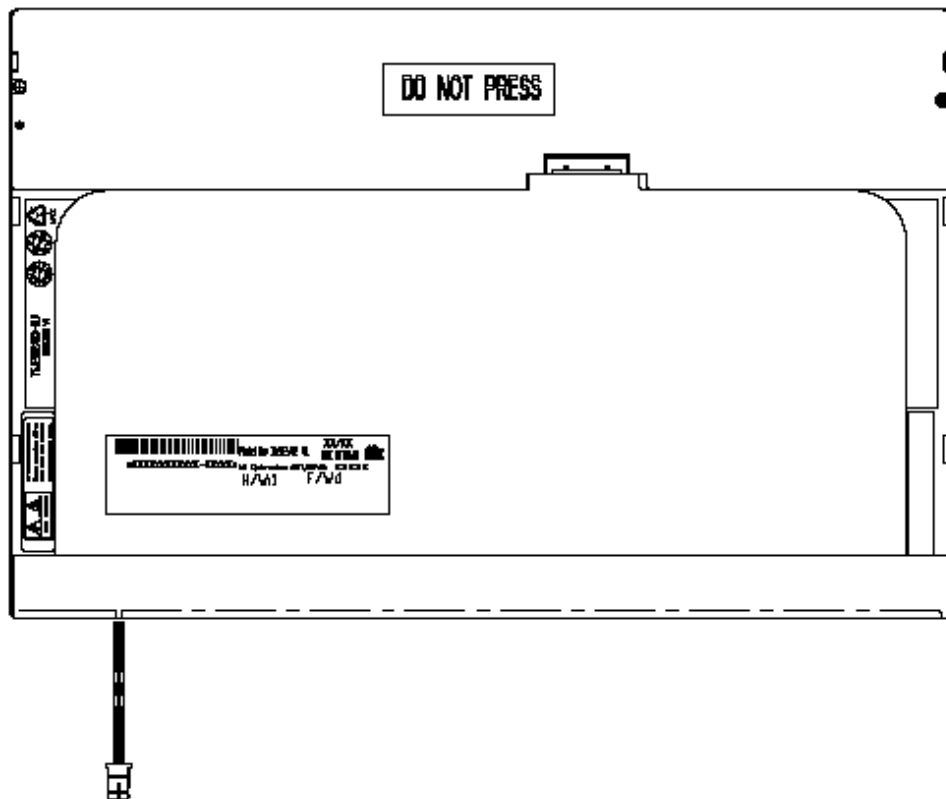
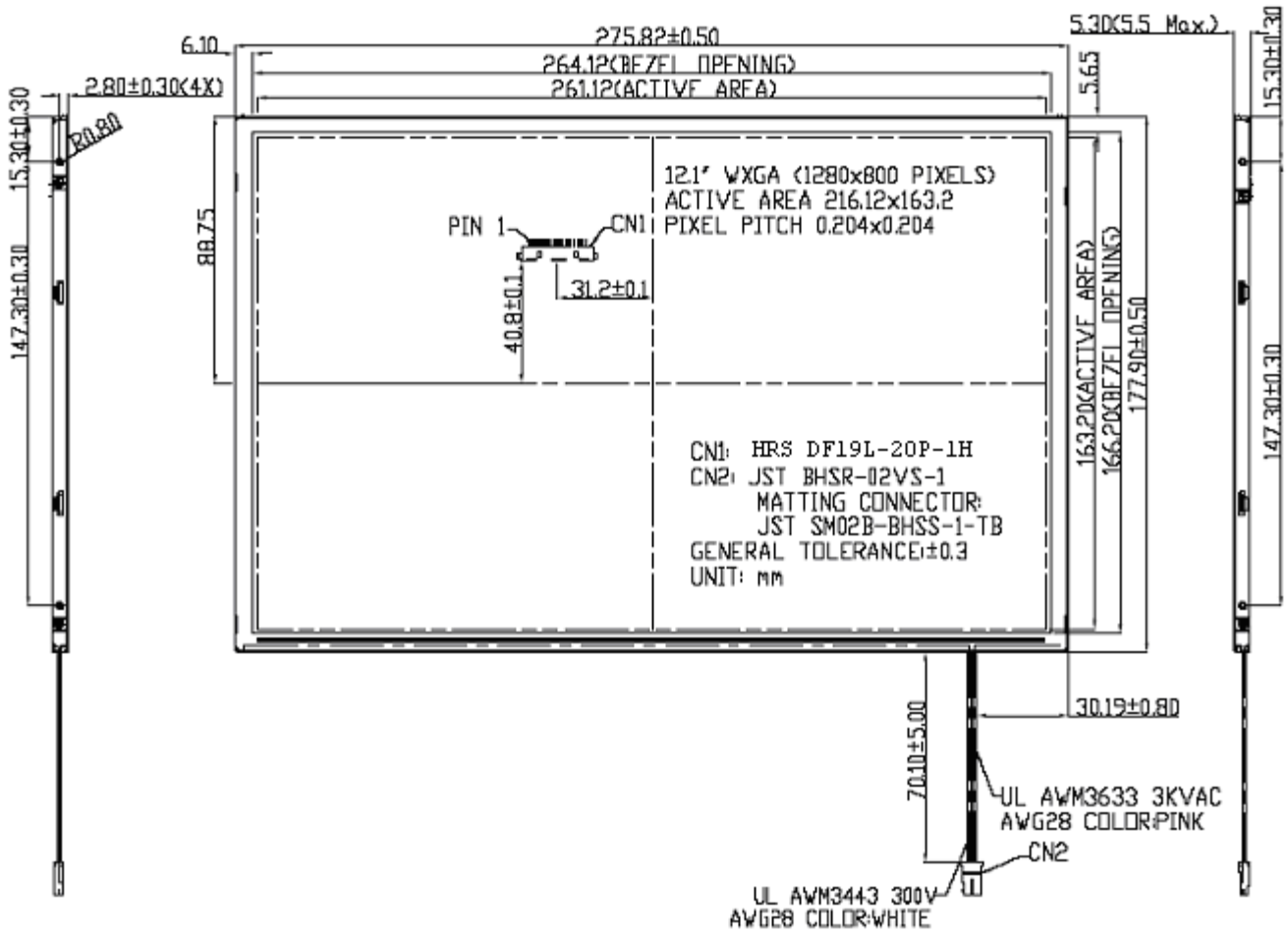
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
 . Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

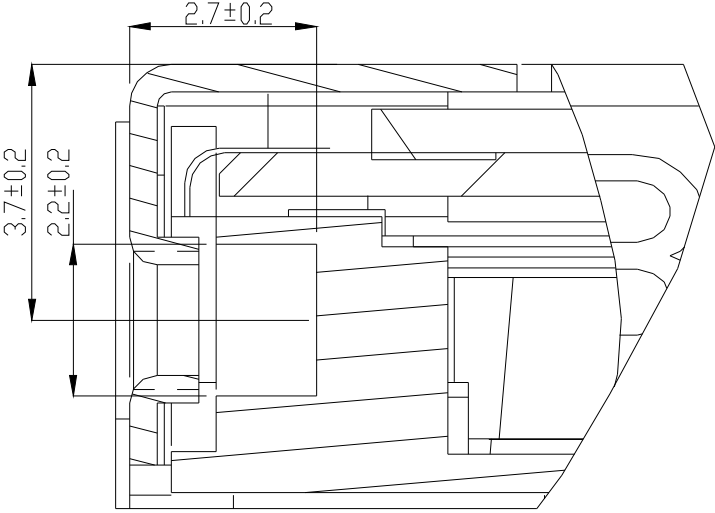


10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.5 mm (See drawing)

Screw hole center location, from front surface = 3.7 ± 0.2 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm



11. Shipping and Package

11.1 Shipping Label Format



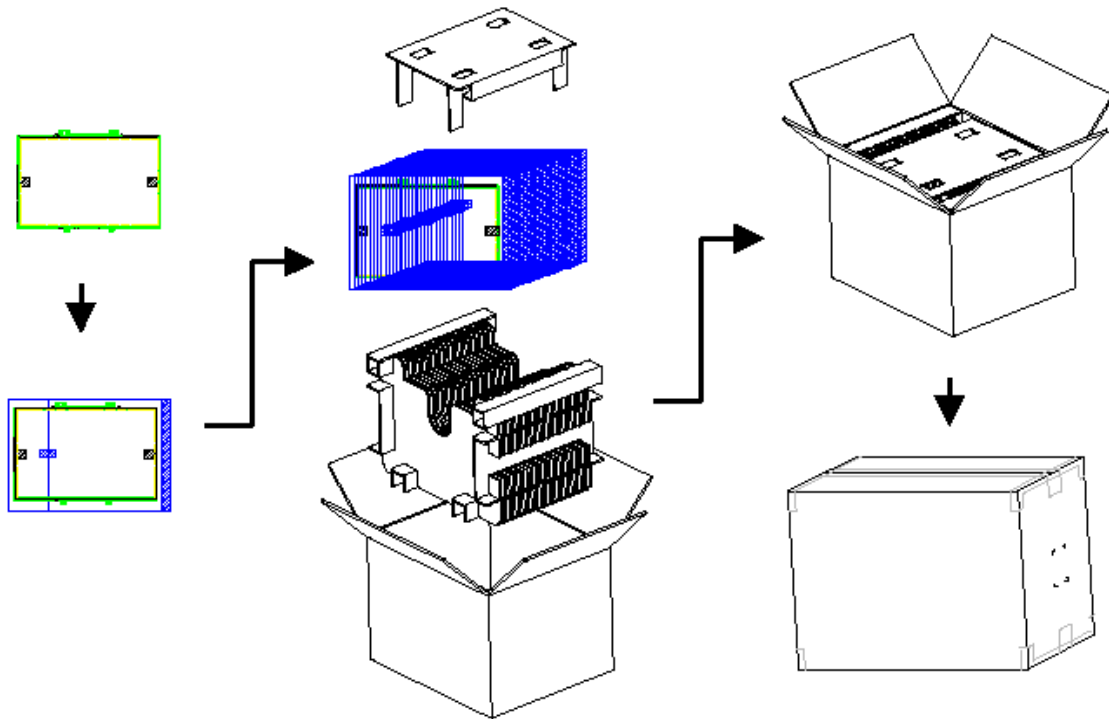
note 1

Note 1:

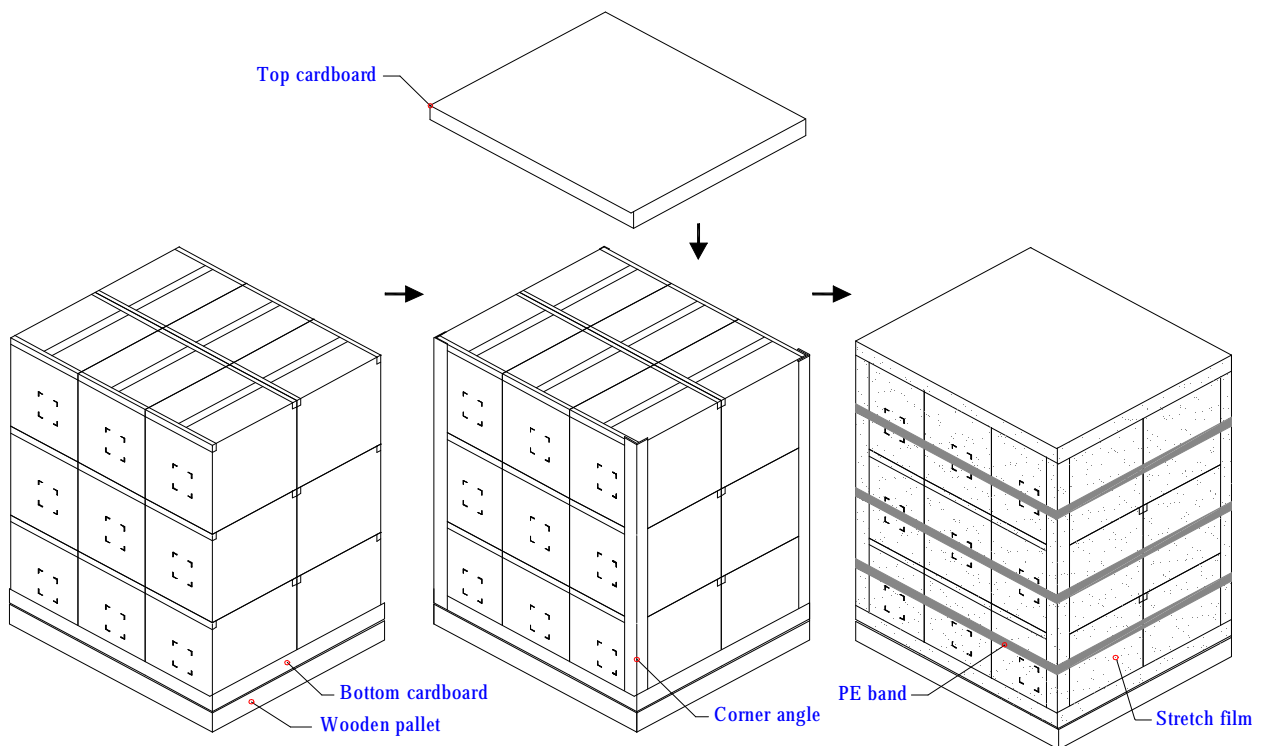
IC Combination	Control Code	H/W
Source IC:NT Gate IC: NT	OAXXX	0A
Source Gate IC: NEC	1AXXX	1A

11.2. Carton package

The outside dimension of carton is 486 (L)mm x 286 (W)mm x 360 (H)mm



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

